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Claims 1-5, 11-17 and 23-25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Haas, U.S. Patent 5,469,284. Claim 6-8 and 18-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Haas in view of Shively, U.S. Patent 5,978,370. Those rejections are respectfully traversed and reconsideration is requested.

As discussed from the bottom of page 2 of the application, an all optical switch addresses the problem of electronic bandwidth, but has difficulty performing the logic needed to route packets or providing the memory required for packet buffering. Also, optical switches typically switch very slowly. In accordance with the present invention, an optical switch operates with a schedule which allows for much slower switching than would be required if the routing were directly determined by the input packets. Reordering units rearrange the order of the data units within data streams to correspond to the schedule of the switch, thus allowing the packets to be appropriately matched to the switch schedule for appropriate routing.

Haas does not suggest claims 1 and 13 because it does not include "an optical switch that operates with a schedule not directly determined by the input stream." Haas describes an optical packet switch that uses two switches, called the "scheduling stage" 16 and the "switch stage" 18. These two stages are connected by delay lines of various lengths. Both switches 16 and 18 are scheduled in direct response to the input stream. Specifically, as disclosed in Figures 3 and 7 and in column 6, line 36, to column 7, line 52, the header of each packet is extracted to determine the requested output port. These output port requests are then scanned in order and an iterative circuit (Figure 7) assigns each to a time slot or column. This assignment schedules both switches since the time slot determines the delay required, and hence the setting of switch 16 during the cycle the packet arrives. The time slot also determines the setting of switch 18 at the time the packet exits the delay line to connect the packet to the address indicated by the packet header. Hence, Haas describes a system where two switches are scheduled in direct response to the input stream; Haas does not suggest claims 1 and 13 which recite "a schedule not directly determined by the input stream."

Haas also does not anticipate claim 25 because it does not include "reordering means for rearranging the order of data units within data streams to correspond to the schedule of the switch

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means." The delay lines 22 of the Haas application do act to reorder the input data stream. However, this reordering is not done to correspond to the schedule of the switch means; that is, the ordering is not computed in response to the schedule. Further, Haas computes the ordering and the switch schedule jointly as described above.

The examiner states: "since the input streams are received by the scheduling stage 18 prior of entering the switch, therefore the operation of the switch is not directly determined by the input streams." However, it can be seen that both the scheduling stage 16 and the switch stage 18 are controlled by control circuit 30 which in turn receives address information from the header detectors 28. See column 5, lines 45-57. The state of the switch stage 18 is directly dependent on the state of the scheduling stage which is in turn directly dependent on the address information extracted from the header detectors. Accordingly, the schedule of each of the stages 16 and 18 is directly determined by the destination addresses of the input stream.

Other claims are also not suggested by Haas. For example, in accordance with claims 11 and 12, the switch schedule is determined by the average load between inputs and outputs. There is no discussion of average load in Haas.

With respect to claims 6-8 and 18-20, which are further rejected in view of Shively, a teaching of a time slot interchanger does not itself suggest the use of such a device to reorder units in accordance with base claims 1 and 13. Shively teaches nothing with respect to the deficiencies of Haas.